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Transformerless Step-Down Integrated Buck Buck-Boost Converter

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***Abstract*—A high step down transformerless integrated buck buck-boost converter is presented in this paper which is suitable for universal line applications (90-270 V_{rms}). The topology integrates a buck converter with a buck-boost converter with low intermediate voltage and output voltage. Buck converter acts as a PFC cell and buck-boost converter as DC/DC cell and as a whole the converter performs power factor correction. The converter is able to achieve efficient power conversion, high power factor and low output voltage under all input and output conditions without step-down transformer due to direct power transfer and sharing of capacitor voltages. The absence of transformer reduces the component count, size and cost of the converter. The circuit is successfully tested using MATLAB/Simulink.**

***Index Terms*— Integrated Buck Buck-Boost converter(IBuBuBo); transformerless; Discontinuous conduction mode (DCM); Power factor correction (PFC).**

I. INTRODUCTION

Single stage ac/dc converters are gaining more attention owing to its low cost, compact size and simple control mechanism. Among existing SS converters, for output voltage regulation most of them consist of boost PFC cell [2], [3] followed by a dc/dc cell. At high-line application their intermediate bus voltage is usually greater than the line input voltage and easily goes beyond 450 V. This high intermediate bus voltage increases component stresses on the dc/dc cell. With a buck or buck-boost converter as dc/dc cell, extremely narrow duty cycle is needed for the conversion. This leads to poor circuit efficiency and limits the input voltage range for getting better performance. Therefore a high step down transformer [6], [7], [8] is usually employed, thus isolation has been done in PFC stage, and the second transformer in the dc/dc cell for the sake of isolation are considered as redundant. Hence, non-isolated ac/dc converter can be employed to reduce unnecessary isolation and improves efficiency of the overall system. Besides, leakage inductance of the transformer causes high spikes on the active switch and conversion efficiency is reduced. To protect the switch, a snubber circuit is usually added but it increases the component count.

To tackle these problems, an effective way is to reduce the bus voltage much below the line input voltage. The converters use different PFC cells to reduce intermediate bus voltage. Among those converters, a transformer is used to achieve low output voltage either in PFC cell or dc/dc cell. Thus the leakage inductance is unavoidable. Converters use a buck boost PFC cell [4], [5] resulting in negative polarity at the output terminal.

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The converter employs resonant technique [9] to further increase the step-down ratio based on a buck converter to eliminate the use of intermediate storage capacitor, apart from reducing the intermediate bus voltage. The converter features with zero-current switching to reduce the switching loss. However, the converter cannot provide hold-up time without the intermediate storage and presents substantial low-frequency ripples on its output voltage.

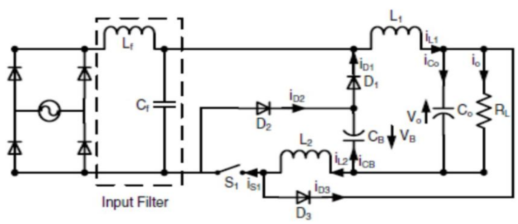
In this paper, an integrated buck buck-boost converter with low output voltage is presented. The converter utilizes a buck converter as a PFC cell and buck boost converter as dc/dc cell. It is able to reduce the bus voltage below the line input voltage effectively and also by sharing voltages between the intermediate bus and output capacitors, further reduction of the bus voltage can be achieved. Therefore, a transformer is not needed to obtain the low output voltage. The converter is also able to achieve:

1) low intermediate bus and output voltages in the absence of transformer;
2) simple control structure with a single-switch;
3) positive output voltage;

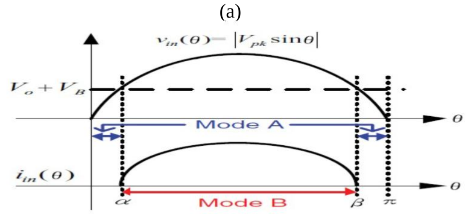
The paper is organized as follows: Integrated buck buck-boost converter circuit configuration and principle of operation is presented in section II. Design consideration is illustrated in section III. Simulation result of integrated buck buck-boost converter is given in section IV. Finally conclusion is stated in section V.

II. Circuit configuration and principle

The Integrated Buck Buck-Boost converter is illustrated in Fig. 1(a). It consists of a buck PFC cell (L_1, S_1, D_1, C_O and C_B) and a buck boost dc/dc cell (L_2, S_1, D_2, D_3, C_O and C_B). Here, L_2 is on the return path of the buck PFC cell, it does not contribute to the cell electrically. Thus L_2 is not considered as part of the PFC cell. Both cells are operated in discontinuous conduction mode (DCM), and therefore no current flows through the inductors L_1 and L_2 at the beginning of each switching cycle t_0. Due to the characteristic of buck PFC cell, there are two operating modes in the circuit. Buck converter operates only when input voltage is greater than output and intermediate bus voltage.



(a)



(b)

Fig. 1(a) Proposed IBuBuBo converter. (b) Input Voltage and Current Waveform

A. Mode A (Buck boost mode - $V_{in}(\theta) \leq V_B + V_O$)

When the sum of intermediate bus voltage V_B, and output voltage V_O is greater than the input voltage V_{in} (θ), the bridge rectifier becomes reverse biased and the buck PFC cell becomes inactive and no line current is present. Only the buck-boost dc/dc cell sustains all the output power to the load. Therefore, two dead-angle zones are present in a half-line period and no input current is drawn as shown in Fig. 1(b).

The circuit operation within a switching period can be divided into three stages.

- Stage 1(period d_1T_S): When switch S_1 is turned ON, diode D_2 becomes forward biased and inductor L_2 is charged linearly by the bus voltage V_B as shown in fig. 2(a). Output capacitor C_O delivers power to the load.
- Stage 2(period d_2Ts): When switch S_1 is switched OFF, diode D_3 becomes forward biased and energy stored in L_2 is released to Co and the load as shown in fig. 2(b).

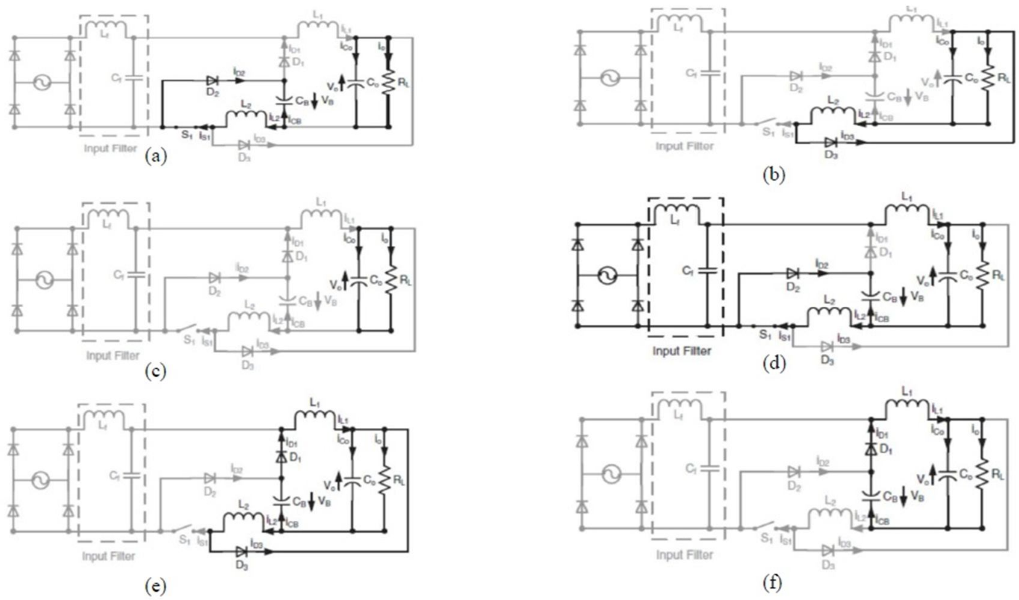


Fig.2. Circuit operation stages of the converter

- Stage 3(period d_3Ts - d_4Ts): The inductor current i_{L2} is totally discharged and only Co sustains the load current as shown in fig. 2(c).

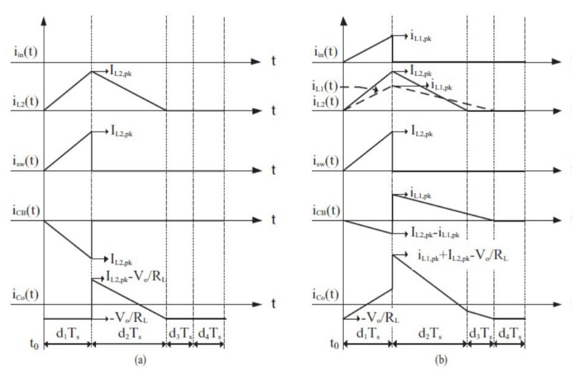


Fig.3 Key waveforms of the circuit

B. Mode B (Buck Mode- $Vin\ (\theta) > V_B + V_O$)

This mode occurs when the sum of the bus voltage and output voltage is smaller than the input voltage. The circuit operation over a switching period can be divided into four stages.

- Stage 1 (period d_1Ts): When switch S_1 is turned ON, diode D2 is forward biased and both inductors L_1 and L_2 are charged linearly by the input voltage minus the sum of the bus voltage and output voltage ($Vin\ (\theta)$ -V_B-Vo) as shown in Fig.2(d).
- Stage 2 (period d_2Ts): When switch S_1 is switched OFF, inductor current i_{L1} decreases linearly to charge C_B and Co through diode D_1 as shown in Fig.2(e). Meanwhile, the energy stored in L_2 is released to Co and the current is supplied to the load through diode D_3. This stage ends once inductor L_2 is fully discharged.
- Stage 3 (period d_3Ts): Inductor L_1 continues to deliver current to Co and the load until its current reaches zero as shown in Fig.2(f).
- Stage 4 (period d_4Ts): Only Co delivers all the output power as shown in Fig.2(c).

Fig. 3 shows the key waveforms of the circuit. Waveforms of Mode A and Mode B are shown in (a) and (b) respectively.

III. DESIGN CONSIDERATIONS

Some assumptions are taken to simplify the circuit analysis, they are:

1) All circuit components are ideal.
2) Input voltage V_{in} (θ) = $V_{pk} \sin\theta$.
3) Both capacitors C_B and C_O are large so that it treated as constant DC voltage source without ripples.

Let consider resonance frequency F_r as 2500Hz. Value of filter inductor and capacitor is calculated by the equation:

$$F_r = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{1}$$

The critical inductances are calculated by using the relation:

$$L_{1-crit} = \frac{R_{L-min} T_S Vpk}{2\pi {V_o}^2}\left[Vpk\left(\frac{\gamma}{2} + \frac{\sin 2\alpha - \sin 2\beta}{4}\right) + V_T(\cos\beta - \cos\alpha)\right] d_{1\_max}^2 \tag{2}$$

$$L_{2\_crit} = \frac{R_{L-min} {V_B}^2 T_S}{2{V_o}^2} d_{1\_max}^2 \tag{3}$$

Where $\alpha = \sin^{-1}\frac{V_T}{V_{pk}}$, $\beta = \pi - \alpha$, $\gamma = \beta - \alpha$

The value of bus capacitance can be calculated from the relation:

$$C_B = \frac{2 * P_{out} * t_{hold-up}}{(V_{B-nominal}^2 - V_{B-min}^2)} \tag{4}$$

The value of output capacitance is calculated by using the relation:

$$C_o = \frac{1}{4fR_L}\left[1 + \frac{1}{\sqrt{2} * Ripplefactor}\right] \tag{5}$$

Due to sharing switch in both cells of converter, the maximum duty cycle of the converter is

$$D = min\left(d_{1-PFC} , d_{1-DC/DC}\right) \tag{6}$$

where $d_{1-PFC} = \frac{V_T}{V_{in}}$, $d_{1-DC/DC} = \frac{V_o}{V_T}$

IV. SIMULATION RESULTS

The performance of the circuit is verified using MATLAB/Simulink. Simulation model for a buck buck-boost converter with universal input voltage range 90-270 V_{rms} and output voltage of 19V DC is shown in Fig. 4. The input power factor of the converter can be viewed on power factor display block.

TABLE I. DESIGN PARAMETERS

PARAMETERS	VALUES
Filter inductance	2mH
Filter capacitance	2µF
Inductance L_1	106µH
Inductance L_2	46µH
Bus capacitance C_B	5mF
Output capacitance C_O	5mF
Switching frequency	20kHz

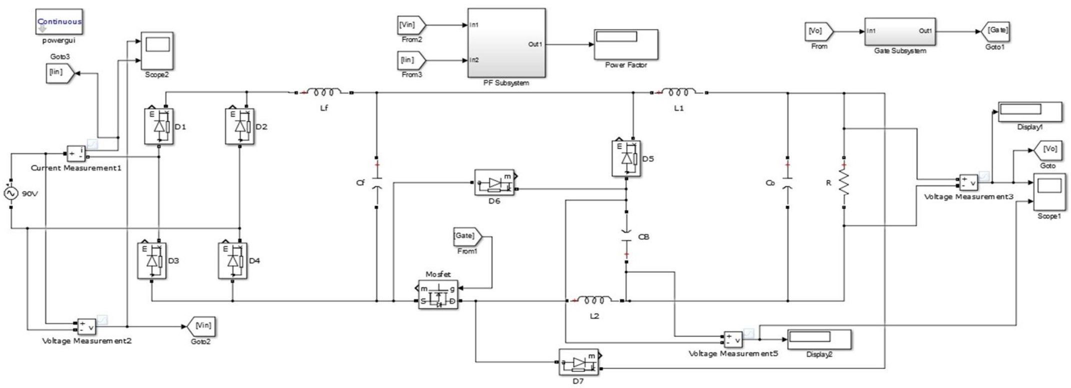


Fig.4. Simulation model of buck buck-boost converter

The control block generates the gate signal for controlling the switch. The rated output voltage of the converter, 19 V is given as the reference voltage. The output voltage is subtracted from the reference value to produce the error signal. This error signal is the input to the PI controller. The controller output is used to maintain the output voltage value close to the reference value. The output of the PI controller is compared with the saw tooth signal in the relational operator block. Whenever the controller output is greater than the ramp signal, a pulse is generated. Thus output voltage is regulated and obtained as 19 V dc under both low and high line conditions. Thus high step down is occurred during both low and high line conditions. Also bus voltage is obtained at 112 V and well below 150 V at high-line condition which leads to increase in circuit efficiency and decrease in the stress on the components. Fig. 6 shows the output and intermediate bus voltages at low line condition. The bus voltage obtained is used to perform mode A operation when no line current is present. Thus the output voltage is stabilized well before the bus voltage reaches the steady state value.

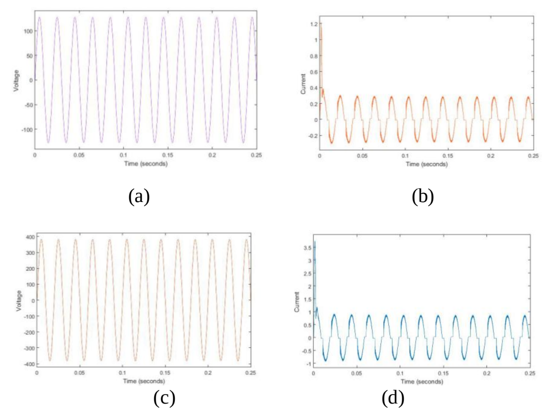


Fig.5 (a) and (b) Input voltage and current at V_{in} = 90V respectively. (c) and (d) Input voltage and current at V_{in} = 270V respectively

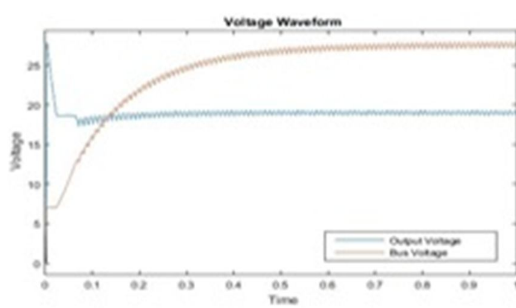


Fig.6 Voltage Waveforms at 90 V_{rms}

IV. CONCLUSION

The Integrated Buck Buck-Boost Converter has been simulated. The intermediate bus voltage of the circuit is maintained below 150 V at all input and output conditions, and is lower than that of the most reported converters. Thus the converter is able to achieve less bus voltage and output voltage without using any resonant converters, high step down transformers etc. Thus unlike all the existing converters, Integrated Buck Buck-Boost converters can reduce the component count and complexity in control and is able to achieve a power factor around 0.97.

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